TMC2361

Flicker Free PC-to-TV Encoder

Features

- Low cost
- 3-line flicker filter
- Minimal external components
- Accepts 640x480 50/60 Hz VGA
- Multiple output standards
- Composite and S-video output formats
- I^2C compatible port and direct controls
- 2x oversampling 9-bit D/A converters
- Auto sync polarity detection
- 64 pin MQFP package
- VGA software for DOS and Windows

Applications

- PC video out
- TV VGA in
- VGA to video converter modules
- Video games

Description

Standard VGA 640x480 50/60 Hz video is converted to NTSC or PAL video by the TMC 2361. A/D converters, flicker filter, video encoder, 2x oversampling D/A converters and control logic are included within a single package. NTSC or PAL video out from a PC may be implemented with minimal external components.

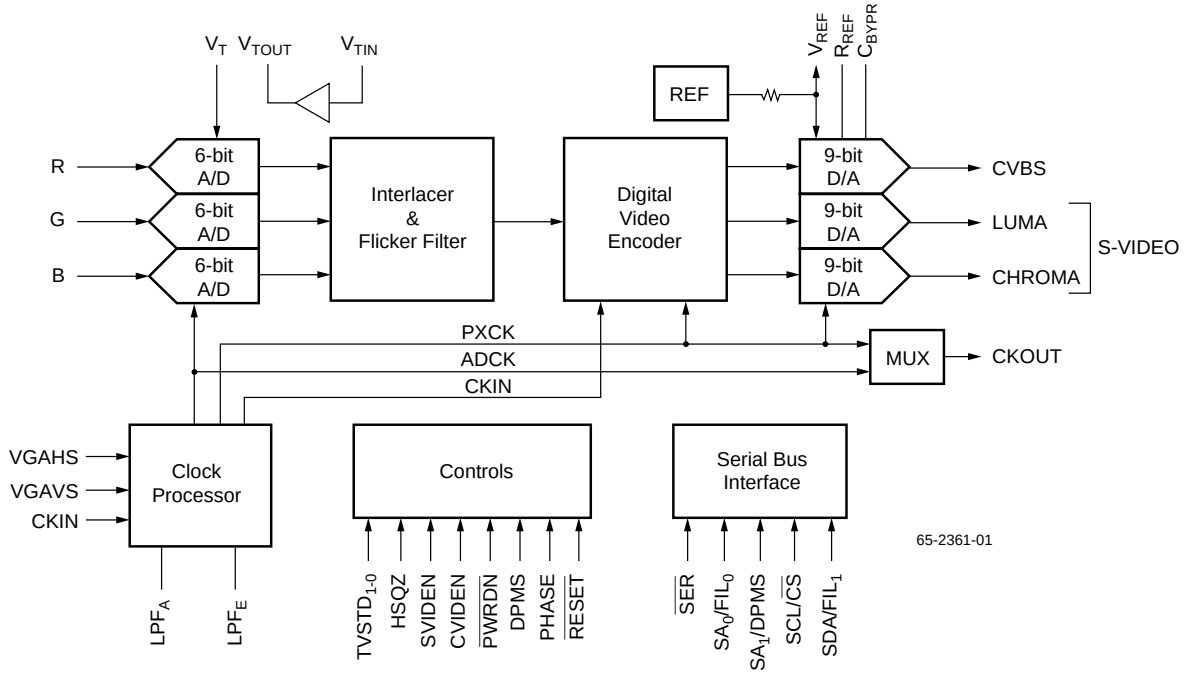
Line-to-line twitter is minimized with the fully-integrated 3-line flicker filter. Composite and S-Video outputs are compliant with SMPTE-170M and CCIR-624 specifications. NTSC and PAL subcarrier frequencies are referenced to a 14.31818 MHz crystal.

Setup is via either an I^2C compatible serial port or directly through pins. Selectable modes are NTSC/NTSC-EIA J/PAL/PALM, 1, 2, 3-line flicker filter, horizontal squeeze (88% scaling), DPMS (VESA display power management) and internal test patterns.

Power is derived from a single +5V supply. Package is a 64-lead Metric Quad Flat Pack (MQFP).

Preliminary Information

Block Diagram



Rev. 0.9.3

Functional Description

Triple 6-bit A/D converters digitize the analog RGB inputs. A 3-line flicker filter band-limits the spatial frequencies of columns of pixels to remove high frequency components such as high-to-low luminance boundaries which will cause flicker on an interlaced TV image. A digital encoder converts the flicker filter output to composite and separate Y/C luminance and chrominance outputs for S-video.

Incoming VGA frame rate must equal outgoing TV field rate. VGA line rate must be twice the outgoing TV line rate. Supported VGA formats are 640x480/60 Hz for NTSC and PAL-M, and 640x480/50 Hz for PAL B/G/H/I.

Nominally, there must be 525 lines per frame for NTSC and 625 lines per frame for PAL. Other modes such as 447 line/ 60 Hz are supported if the line rate is close to 31.469 kHz and the TV will accept the accelerated vertical refresh rate.

Input Section

Analog VGA signals are digitized by three 6-bit A/D converters, operating at rates of up to 25 Ms/s. Incoming signal range is 0 to 700 mV established by the reference voltage, V_{RT}.

V_T, the A/D converter reference voltage is supplied by an on-chip voltage follower. V_T is set by V_{TIN}, which may be varied to accommodate different input levels.

Clock Processor

Either positive or negative sync polarity is accepted. Two phase-locked loops synthesize clocks from the VGA Horizontal Sync signal. One loop generates the A/D sample clock, ADCK. A second PLL generates the digital encoder clock, PXCK. Both PLLs are referenced to the leading edge of horizontal sync, thus avoiding re-centering the image if sync polarity is inverted.

A stable reference for NTSC or PAL subcarrier generation is derived from a 14.31818 MHz TTL clock applied to pin CKIN.

To synchronize the video encoder, vertical timing is derived from VGAVS, the VGA vertical sync signal. VGAHS and VGAVS signals of either polarity are accepted.

VESA Display Power Management Signaling functions may be enabled with the DPMS pin. DPMS STAND-BY and SUSPEND modes set the processor to sleep and blank the screen. DPMS active sets the processor, A/Ds and D/As to sleep with a blanked screen.

Flicker Filter

Flicker that will be visible on a TV display may be traded for vertical resolution by selecting either 1, 2, or 3-line filtering. Setup is via the serial port or through pins. A fourth mode, Color Bars, is useful for setup of video levels or self test.

Video Encoder

$TVSTD_{1-0}$ pins or register bits select the TV standard to be either NTSC, PAL or PAL-M.

NTSC (SMPTE 170M) and PAL (CCIR 624) video signals are produced by three 9-bit D/A converters. Each D/A converter can drive a 37.5Ω load (double-terminated 75Ω line) or a 75Ω load to minimize power dissipation. Digital 2X oversampling minimizes sinx/x distortion, facilitating use of low-cost or no output filters.

Encoder Output Current

Output current is established by V_{REF} and an external resistor connected between R_{REF} and ground. The internal V_{REF} may be overridden by an external voltage.

To minimize DAC noise, a bypass capacitor must be connected from C_{BYPR} to an adjacent V_{DDA} pin.

Control Mode Selection

Internal control bits may be accessed in two ways, selectable by the $\overline{SER}$ pin. With $\overline{SER}$ = LOW, access is through the serial port. With $\overline{SER}$ = HIGH, access is through pins with $\overline{CS}$ acting as a latch control pin.

With the serial bus enabled, internal registers are programmed via SCL and SDA. Bit assignments within the registers are shown in Table 12.

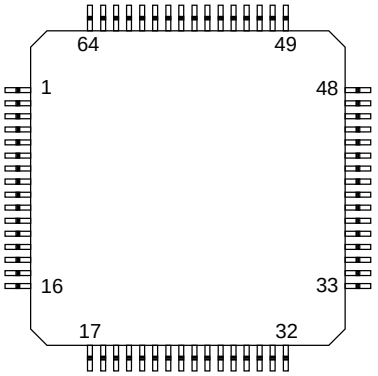
With the serial bus disabled, HQSZ, TVSTD0, TVSTD1, DPMS and $\overline{RESET}$ may be latched by $\overline{CS}$.

Serial Control Port

Five registers are accessible via the I^2C compatible serial port. All control functions may be accessed by setting bits in registers VGA0, VGA1 and VGA2. Revision ID and Part ID may be read from two other registers. To access a register, the pointer register must be loaded with the target register address.

Pin Assignments

64-Lead MQFP Package



65-2361-02

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	SDA, FIL1	17	RREF	33	LPFP	49	—
2	VDD	18	VREF	34	VSSPLLP	50	—
3	VSS	19	VDDA/D	35	VSSPLLA	51	SA1, DPMS
4	VDD	20	VSSA/D	36	LPFA	52	CKOUT
5	SCL, $\overline{CS}$	21	R	37	VDDPLLP	53	$\overline{RESET}$
6	CVIDEN	22	VDDA/D	38	VDDPLLA	54	VSSQ
7	SVIDEN	23	VDDA/D	39	CKIN	55	VSS
8	VDDD/A	24	G	40	VGAHS	56	VDD
9	VDDD/A	25	VSSA/D	41	VGAVS	57	VDDQ
10	VDDD/A	26	VT	42	SAO,FIL0	58	$\overline{PWRDN}$
11	CHROMA	27	VTOUT	43	PHASE	59	TVSTD1
12	CBYPR	28	VTIN	44	VSS	60	TVSTD0
13	LUMA	29	VSSA/D	45	VSS	61	VDD
14	VSSD/A	30	B	46	VDD	62	—
15	VSSD/A	31	VDDA/D	47	VDD	63	—
16	CVBS	32	VSSA/D	48	$\overline{SER}$	64	—

Pin Descriptions

Pin Name	Pin Number	Type/Value	Description
Clocks			
CKIN	39	TTL	**Subcarrier Reference Clock.** Input from 14.31818 MHz ±50 ppm. external oscillator. Subcarrier frequency is derived from this clock.
VGAHS	40	$CMOS_{SP}$	**VGA Horizontal Sync Input.** Either polarity VGAHS is accepted, active HIGH or active LOW.
VGAVS	41	$CMOS_{SP}$	**VGA Vertical Sync Input.** Either polarity VGAVS is accepted, active HIGH or LOW.
CKOUT	52	TTL	**Clock Out.** Default is PXCK. Select either PXCK or ADCK by programming register 2.
LPF_A	36	—	**A/D Clock Phase-Locked Loop Filter Node.** External RC network is connected here.
LPF_P	33	—	**Encoder Clock Phase-Locked Loop Filter Node.** External RC network is connected here.
Controls			
$TVSTD_{1-0}$	59,60	$CMOS_P$	**Video Output Standard Select ($\overline{SER}$ = H, $\overline{CS}$ = H).** Preprogrammed into the TMC2361 are timing, subcarrier frequency and phase parameters corresponding to worldwide NTSC and PAL standards. $TVSTD_{1-0}$ select one of four sets of parameters to set up the encoder. Frame rate of the graphics source must be twice the frame rate of the selected video standard.
DPMS (SA_1)	51	$CMOS_P$	**Display Power Management ($\overline{SER}$ = H, $\overline{CS}$ = H).** DPMS = H, enables partial power down modes in response to missing VGAHS and VGAVS signals. DPMS = L, disables response VGAHS and VGAVS signals and absence of VGAHS or VGAVS signals blanks the screen BLUE.
FIL_0 (SA_0)	42	$CMOS_P$	**Flicker Filter Pin 0 ($\overline{SER}$ = H, $\overline{CS}$ = H).** In conjunction with FIL_1, FIL_0 selects one of three filter modes or a color bar test pattern.

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Pin Descriptions (continued)

Pin Name	Pin Number	Type/Value	Description
FIL_1 (SDA)	1	$CMOS_{SP}$	**Flicker Filter Pin 1 ($\overline{SER}$ = H, $\overline{CS}$ = H).** In conjunction with FIL_0, FIL_1 selects one of three filter modes or a color bar test pattern.
$\overline{PWRDN}$	58	$CMOS_P$	**Power-Down Control ($\overline{SER}$ = H, $\overline{CS}$ = H).** HIGH enables TMC2361, LOW minimizes power consumption. D/A converters and clocks are disabled. Set-up states are retained and are restored when $\overline{PWRDN}$ transitions to HIGH.
$\overline{RESET}$	53	$CMOS_P$	**Reset ($\overline{SER}$ = H, $\overline{CS}$ = H)** Initializes internal registers. Connect via 0.1µF capacitor to ground.
PHASE	43	$CMOS_P$	**A/D Sampling Phase.** Selects either negative or positive ADCK edge for A/D conversion.
$\overline{CS}$ (SCL)	5	$CMOS_{SP}$	**Chip Select. ($\overline{SER}$ = H).** LOW latches control inputs. HIGH sets latches transparent.
Encoder Controls			
SVIDEN	7	$CMOS_P$	**S-Video Enable.** HIGH enables LUMA and CHROMA S-video outputs. LOW disables S-video D/A converters to minimize current.
CVIDEN	6	$CMOS_P$	**Composite Video Enable.** HIGH enables the CVBS output. LOW disables the CVBS D/A converter to minimize current.
A/D Converter Interface			
R, G, B	21, 24,30	700 mV	**Analog Red, Blue and Green Inputs.** Incoming VGA signals. Nominal voltage range is 0.0 to +0.7 Volts.
V_{TIN}	28	750 mV	**Top Reference Voltage Buffer Input.** Input to voltage follower supplying V_{TOUT}.
V_{TOUT}	27	750 mV	**Top Reference Voltage Buffer Output.** Output from voltage follower. Connect to V_T.
V_T	26	750 mV	**A/D Converter Top Reference Voltage.** Supplies current to A/D converter reference resistors. Connect to V_{TOUT}. Range is 0.5–2.0 volts.
Video Outputs			
CVBS	16	1000 mV	**Composite Video Output.** NTSC/PAL base-band composite video output with blank and sync and subcarrier. Drive level is 1 Volt peak-peak video into a 37.5 Ohm load.
LUMA	13	1000 mV	**Luma Video Component.** Analog monochrome component of S-video output. Can drive 1 Volt peak-peak video into a 37.5 Ohm load.
CHROMA	11	1000 mV	**Chromae Video Component.** Analog chroma component of S-video output. Can drive a 37.5 Ohm load. The CHROMA signal, when combined with the LUMA output signal, comprises an S-Video two-wire video signal.
Voltage Reference			
V_{REF}	18	+1.23 V	**Voltage Reference Input/Output.** If unconnected, except for a 0.1µF capacitor internal 1.23 Volt band-gap reference will be supplied to the three D/A Converters . An external 1.2 volt reference connected to the V_{REF} pin, will override the internal voltage reference.
R_{REF}	17	392/787Ω	**Reference Resistor.** Sets the current range of D/A converters. Connected resistor between R_{REF} and ground. Use 392Ω for a 37.5Ω load and 787Ω for a 75Ω load.

Pin Descriptions (continued)

Pin Name	Pin Number	Type/Value	Description
C_{BYPR}	12	0.1 µF	**Bypass Capacitor.** Connect a 0.1 µF capacitor between C_{BYPR} and V_{DDA} to reduce noise at the D/A outputs.
Serial Port			
SA_1 (DPMS)	51	$CMOS_P$	**Serial Data Address Bit 1. ($\overline{SER}$ = L).** In conjunction with SA_1, SA_0 selects one of four addresses for the TMC2361.
SA_0 (FIL_0)	42	$CMOS_P$	**Serial Data Address Bit 0. ($\overline{SER}$ = L)**. In conjunction with SA_0, SA_1 selects one of four addresses for the TMC2361.
SDA (FIL_1)	1	$CMOS_{SP}$	**Serial Data.**
SCL ($\overline{CS}$)	5	$CMOS_{SP}$	**Serial Clock. ($\overline{SER}$ = L)**
$\overline{SER}$	48	$CMOS_P$	**Serial Port Select.** $\overline{SER}$ = L enables the serial port interface. $\overline{SER}$ = H, disables the serial interface and enables direct access control pins.
Power and Ground			
V_{DD}	2, 4, 46, 47, 56, 61	+5.0 V	**Digital Power.** Supplies +5V power to internal digital circuits.
V_{DDQ}	57	+5.0 V	**Digital Power, Driver.** Supplies +5V power to digital driver circuits.
V_{DDPLLA}	38	+5.0 V	**ADCK Phase-Locked Loop Power**. Filtered +5 volt power for ADCK phase locked loop.
V_{DDPLLP}	37	+5.0 V	**PXCK Phase-Locked Loop Power.** Filtered +5 volt power for PXCK phase locked loop.
$V_{DDD/A}$	8, 9, 10	+5.0 V	**D/A Converter Power.** Supplies +5V power to digital-to-analog converters. All power voltages must originate from the same source.
$V_{DDA/D}$	19, 22, 23, 31	+5.0 V	**A/D converter Power.** Supplies +5V power to analog-to-digital converters. All power voltages must originate from the same source.
V_{SS}	3, 44, 45, 55	0 V	**Digital Ground.** Ground point for internal digital circuits. Connect grounds to common plane.
V_{SSQ}	54	0 V	**Digital Driver Ground.**
$V_{SSD/A}$	14, 15	0 V	**D/A Converter Grounds.**
$V_{SSA/D}$	20, 25, 29, 32	0 V	**A/D Converter Grounds.**
V_{SSPLLA}	35	0 V	**Phase-locked loop Ground.** Ground ADCK phase locked loop.
V_{SSPLLP}	34	0 V	**Phase-locked loop Ground.** Ground for PXCK phase locked loop.

Notes:
1. $CMOS_P$ = CMOS with light pull-up
2. $CMOS_S$ = CMOS with Schmitt trigger
3. $CMOS_{SP}$ = CMOS with Schmitt trigger and light pull-up

Preliminary Information

Control Modes

Direct Pin Access

With the $\overline{SER}$ = HIGH, some functions may be controlled directly through pins. These include:

- $TVSTD_{1-0}$ – selection of NTSC or PAL TV formats
- $\overline{PWRDN}$ – power down the TMC2361.
- $\overline{RESET}$ – reset all internal counters and registers.
- DPMS – enable display power management through sync pulses
- FIL_{1-0} – Filter mode selection pins

With $\overline{CS}$ = HIGH, the TMC2361 responds immediately to the above inputs. With $\overline{CS}$ = LOW, these inputs are latched.

Serial Bus Interface

With $\overline{SER}$ = LOW, all setup functions are accessible through the serial interface. Five registers, 0,1,2,5 and 6 are accessible as shown in Table 1. Registers 3-4 are reserved.

Table 1. Serial Bus Registers

Pointer Register Value	Register
x	Pointer Register
0	VGA Register 0
1	VGA Register 1
2	VGA Register 2
5	Part ID (61h)
6	Revision ID (≥1Bh)

To access an individual data register (VGA or ID), a serial bus read or write cycle must be initiated. Note that registers 5 and 6 are read only and that some register bits are reserved.

To access registers in sequence, the pointer register must be loaded with 00h. Then, a series of register reads or writes will access the registers in sequence from 0 through 6.

Functions of the control register bits are shown in Table 2 and bit assignments are defined in the Control Register Definitions section.

Table 2. Control Register Map

Bit #	Name	Function
Filter and Test Pattern Register (reg. 0)		
7-5	RGB	RGB Fields
4-3	VIDEO	VGA or Test Pattern input
2-1	FIL	Flicker Filter Mode
0		(reserved)
Encoder Control Register (reg. 1)		
7	—	Reserved
6	—	Reserved
5-4	TVSTD	NTSC or PAL TV standard
3	PWRDN	Power Down
2	DPMS	Display Power Management Signaling
1	DISSVID	Disable S-video output
0	DISCVID	Disable composite video output
Reset Register (reg. 2)		
3	CKSEL	Clock Select
7-4, 2-0	—	Reserved (set LOW)

Control Register Definitions

Filter and Test Pattern Register (0)

7	6	5	4	3	2	1	0
R	G	B	VIDEO		FIL		(reserved)

Reg	Bit#	Bit Name	Description
0	7	R	**Red.** Foreground color select for test patterns.
0	6	G	**Green.** Foreground color select for test patterns.
0	5	B	**Blue.** Foreground color select for test patterns.
0	4-3	VIDEO	**Video source.** Selects between video output converted from VGA input and internally generated test patterns. 0 0 Normal video converted from VGA 0 1 Color Bars 1 0 + symbol superimposed on complementary 1 1 Flat field with color selected by RGB bits
0	2-1	FIL	**Filter mode**: 0 0 3-line filter 0 1 pass through (no filtering) 1 0 2-line filter 1 1 3-line filter (repeated)
0	0	-	Reserved.

Encoder Control Register(1)

7	6	5	4	3	2	1	0
HQSZ	(reserved)	TVSTD		PWRDN	DPMS	DISSVID	DISCVID

Reg	Bit#	Bit Name	Description
1	7–6	—	**Reserved.** Set LOW.
1	5-4	TVSTD	**TV standard.** Select from: 1 1 NTSC 1 0 NTSC-EIA 0 1 PAL 0 0 PAL M
1	3	PWRDN	**Power down**. LOW is normal operation. HIGH minimizes power consumption. Serial port remains active.
1	2	DPMS	**Display power management signaling**. LOW enables blue video if either horizontal or vertical sync are missing. HIGH suspends chip operation if either horizontal or vertical sync is missing; if both horizontal and vertical sync are missing sleep is initiated to minimize power.
1	1	DISSVID	**Disable S-video**. LOW enables the S-video output. HIGH disables the S-video output.
1	0	DISCVID	**Disable C-video**. LOW enables the C-video output. HIGH disables the C-video output.

Reset Control Register(2)

7	6	5	4	3	2	1	0
0 (reserved)	0 (reserved)	0 (reserved)	0 (reserved)	CKSEL	0 (reserved)	0 (reserved)	0 (reserved)

Reg	Bit#	Bit Name	Description
2	3	CKSEL	**Clock out select.** LOW selects PXCK. HIGH selects ADCK

Part Identification Register(5) (Read Only)

7	6	5	4	3	2	1	0
MSB							LSB

Reg	Bit#	Bit Name	Description
5	7-0	PARTID	**Part identification.** When read, returns, PARTID = 61.

Revision Identification Register(6) (Read only)

7	6	5	4	3	2	1	0
MSB							LSB

Reg	Bit#	Bit Name	Description
6	7-0	REVID	**Revision identification.** When read, returns revision number beginning with REVID = 1B.

Clocks

There are three internal clocks, CKIN, ADCK, and PXCK. CKIN is the 14.31818 MHz reference clock from which the chroma subcarrier data is synthesized. ADCK is the clock for the A/D. PXCK is the encoder clock for sequencing data to the D/A converters at a 2X rate. By programming register 2, either ADCK or PXCK can be connected to the CKOUT pin. PXCK is the default.

Reference Clock (CKIN)

Accuracy of the PAL/NTSC subcarrier is determined by the precision of the 14.31818 MHz reference signal applied to CKIN. TV receivers are designed to accept ±300 Hz deviation from the subcarrier frequency. CKIN should be derived from a crystal with better than 50 ppm accuracy.

A/D Clock (ADCK)

ADCK is the analog-to-digital converter clock which is derived from incoming VGA horizontal sync (VGAHS) by a phase-lock loop (PLL). ADCK frequency is set by a programmable divide-by-N counter where N is the number of A/D samples between the horizontal sync pulses in each VGA line. $TVSTD_{1-0}$ register bits or pins set the value of N.

Table 3. VGA A/D Clock

Television Standard	$TVSTD_{1-0}$	ADCLK Freq. (MHz)	N
NTSC	1x	25.175	800
PAL640	01	25.250	808
PALM	00	25.175	800

Pixel Clock (PXCK)

PXCK is the video encoder clock which is derived from the incoming VGA HSYNC signal by a second phase-lock loop. Clock frequency is set by a programmable divide-by-M counter. M is the number of encoder samples between horizontal sync pulses. With 2x oversampling, the pixel rate is twice the TV square pixel rate. If horizontal squeeze (HSQZ) is selected (NTSC & PALM only) then the PXCK frequency is increased.

Table 4. NTSC and PAL Pixel Clocks

Television Standard	Line Rate (kHz)	Pixel Rate (MHz)	PLL M
NTSC & PALM	15.734	24.540	780
PAL	15.625	29.500	944

Digitizing

A/D Converter Reference

An on-chip voltage follower is included to supply current to the reference V_T. A stable voltage source greater than the input peak amplitude must be connected to V_{TIN}. V_T must be de-coupled with a 0.1µF capacitor to ground.

Input Signal Conditioning

A/D performance is optimized by driving the RGB video inputs from a source with 200 ohm or less resistance.

Input Format Selection

One of three input VGA formats can be accepted by setting the $TVSTD_{1-0}$ inputs as shown in Table 7. Each VGA input option corresponds to a VGA active video area, frame rate and line rate with a corresponding TV output format.

Table 5. VGA Input Formats

$TVSTD_{1-0}$	H x V Input Pixels	Frame Rate (Hz)	Line Rate (kHz)
1x	640 x 480	59.94	31.469
01	640 x 480	50	31.250
00	640 x 480	60	31.469

Flicker Filter

Flicker artifacts can be eliminated by selecting one of three vertical filter modes, which trade-off vertical resolution against flicker. Without the flicker filter, one contrasting VGA line may be encoded into one field of the TV video, which will flicker at 30 Hz with NTSC and 25 Hz with PAL.

Filter mode may be selected via the serial bus serial port or control pins. With $\overline{SER}$ = LOW, FIL bits in register 0 set the mode. Alternatively, with $\overline{SER}$ = HIGH, pins FIL0 and FIL1 set the mode. One of three flicker filter modes or color bars may be selected.

Table 6. Flicker Filter Selection with FIL_{1-0} pins

FIL1	FIL0	Output	Filter
0	0	Video Input	3-line
0	1	Video Input	pass through
1	0	Video Input	2-line
1	1	Color Bars	3-line

Video Encoder

Architecture of the video encoder is similar to the Raytheon TMC2490. For block diagram details and performance of the luminance and chrominance digital filters, refer to the TMC2490 data sheet.

2x Oversampling

Performance improvement with 2x oversampling is shown in Figure 1 for NTSC and in Figure 2 for PAL. High frequency response is lifted 3 dB for NTSC and 2dB for PAL. With 2x oversampling, for most applications, a sinx/x reconstruction filter can be omitted.

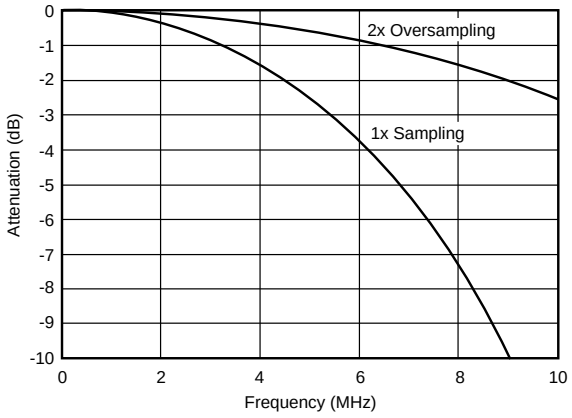

Figure 1. 24.54 MHz 2x oversampling reduces NTSC sinx/x loss

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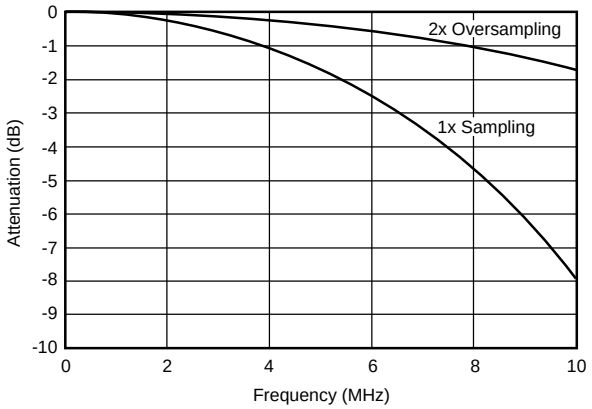

Figure 2. 29.5 MHz 2x oversampling reduces PAL sinx/x loss

Television Standard Selection

NTSC and PAL standards are preprogrammed into the TMC2361 to preset horizontal and vertical timing, subcarrier frequency, and chrominance phase. Frame rate of the VGA source must match the field rate of the selected video standard.

Table 7 shows how the TVSTD1-0 pins select the TV output format.

Table 7. TV Format selection

$TVSTD_{1-0}$	Television Standard	Video Field Rate
11	NTSC	59.94 Hz
10	NTSC-EIA	59.94 Hz
01	PAL/B, G, I	50 Hz
00	PAL/M	60 Hz

Power Management

Power-Down Mode

Power-down eliminates current drain by the D/A converters, V_T voltage follower and clock outputs. With $\overline{PWRDN}$ = HIGH, all outputs are enabled. If $\overline{PWRDN}$ = LOW, all outputs are disabled including the CKOUT, V_{TOUT} and D/A converters.

Display Power Management Signaling (DPMS)

Operational state of the TMC2361 is controlled by the pulse activity on VGAHS and VGAVS. DPMS = H enables Display Power Management compliant with VESA DPMS Proposal 1.0.

Table 8 shows how the TMC2361 responds. Quiescent VSYNC or HSYNC is detected on the second missing VSYNC or HSYNC pulse.

Serial Control Port (R-Bus)

When $\overline{SER}$ is LOW, a 2-wire serial control interface is active. Up to four TMC2361 devices may be connected to the 2-wire serial interface with each device having a unique address. (see Table 9)

Two signals comprise the bus: clock (SCL) and bi-directional data (SDA). The TMC2361 acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on the SCL/$\overline{CS}$ and SDA/R/$\overline{W}$ pins must be pulled HIGH by external resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL = L. An SDA transition while SCL = H is interpreted as a start or stop signal.

There are five steps within a serial bus cycle:

1. Start signal
2. Slave address byte
3. Pointer register address byte
4. Data byte to read or write
5. Stop signal

When the serial interface is inactive (SCL = H and SDA = H) communications are initiated by sending a start signal. The start signal (Figure 3, left waveform) is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is imminent.

The first eight bits of data transferred after a start signal comprise a seven bit slave address and a single R/W bit. As shown in Figure 4, the R/W bit indicates the direction of data transfer, read from or write to the slave device. If the transmitted slave address matches the address of the TMC2361

Table 8. Display Power Management Signaling States

VGAHS	VGAVS	TMC2361 State	
		DPMS = L	**DPMS = H**
Active	Active	Active video	Active video
Quiescent	Active	Image blanked blue	Image blanked black
Active	Quiescent	Image blanked blue	Image blanked black
Quiescent	Quiescent	Image blanked blue (memory off)	Image blanked black (memory, A/Ds and D/As off)

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(set by the state of the SA_0 and SA_1 input pins in Table 9), the TMC2361 acknowledges by bringing SDA LOW on the 9th SCL pulse (see Figure 5). If the addresses do not match, the TMC2361 does not acknowledge.

For each byte of data read or written, the MSB is the first bit of the sequence.

Table 9. Serial Port Addresses

A6	A5	A4	A3	A2	A1 (SA1)	A0 (SA0)
0	0	0	1	1	0	0
0	0	0	1	1	0	1
0	0	0	1	1	1	0
0	0	0	1	1	1	1

Data Transfer via Serial Interface

If a slave device, such as the TMC2361 does not acknowledge the master device during a write sequence, SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the TMC2361 during a read sequence, the TMC2361 interprets this as “end of data.” SDA remains HIGH so the master can generate a stop signal.

To write data to a specific TMC2361 control register, the 8-bit pointer must be loaded with the address of the target control register after the slave address has been established. Value of the pointer is the base address for subsequent write operations. The pointer address auto-increments after each control register data transfer. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 6 and send an acknowledge signal, ACK.

Data is read from the control registers of the TMC2361 in a similar manner, except that two data transfer operations are required:

1. Write the slave address byte with bit R/W = L.
2. Write the pointer byte.
3. Write the slave address byte with bit R/W = H
4. Read the control register indexed by the pointer.

Preceding each slave write, there must be a start cycle. Following the pointer byte there should be a stop cycle. Sequential registers may be accessed by repeated read cycles since pointer auto-increments after each byte transfer. After the last read, there must be a stop cycle comprising a LOW-to-HIGH transition of SDA while SCL is HIGH (see Figure 3, right waveform)

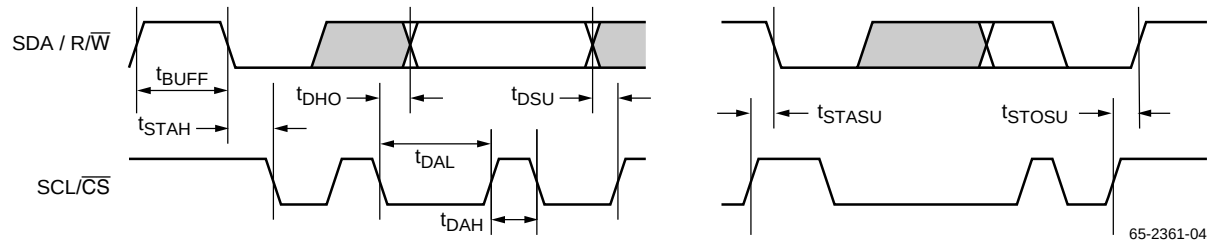


Figure 3. Serial Port Read/Write Timing

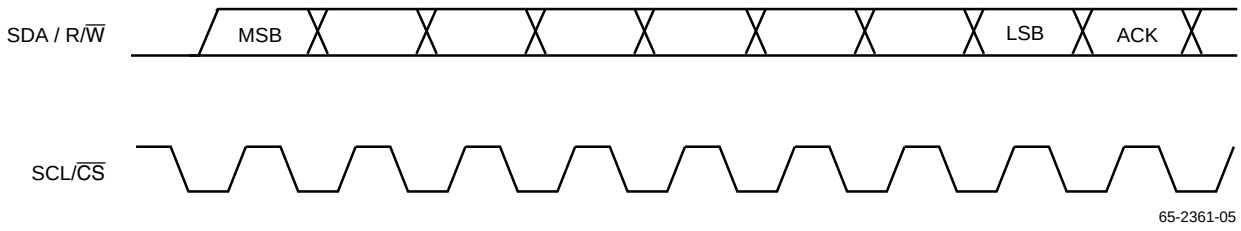


Figure 4. Serial Interface – Typical Byte Transfer

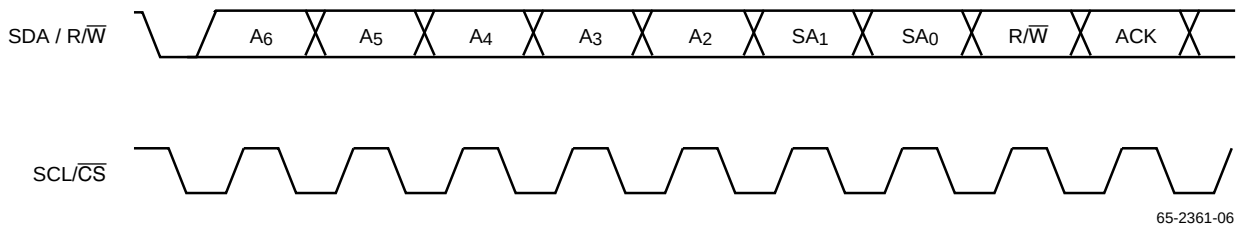


Figure 5. Slave Address with Read/Write Bit

Preliminary Information

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Examples below show how serial bus cycles can be linked together for single and multiple register read and write access cycles. For sequential register accesses, each ACK handshake initiates further SCL clock cycles from the master to transfer the next data byte.

Write to one control register

- Start signal
- Slave address byte (R/W bit = LOW)
- Pointer address byte
- Data byte to register
- Stop signal

Write to two consecutive control registers

- Start signal
- Slave address byte (R/W bit = LOW)
- Pointer address byte
- Data byte to register
- Data byte to register (pointer address + 1)
- Stop signal

Read from one control register

- Start signal
- Slave address byte (R/W bit = LOW)
- Pointer address byte
- Stop signal
- Start signal
- Slave address byte (R/W bit = HIGH)
- Data byte from register
- Stop signal

Read from two consecutive data registers

- Start signal
- Slave address byte (R/W bit = LOW)
- Pointer address byte
- Stop signal
- Start signal
- Slave address byte (R/W bit = HIGH)
- Data byte from pointer address
- Data byte from (pointer address + 1)
- Stop signal

Video Formats

Incoming VGA Formats

Vertical timing must be set for 525 lines in the NTSC mode and 625 lines for PAL. Although the TMC2361 will respond to other line counts such as 449-line 70 Hz, TV sets and monitors may not correctly lock to off-standard video or the image may be shifted.

Table 10 and Table 11 show expected timing formats for NTSC and PAL sources of VGA. For the 2361 to function correctly, both the vertical and horizontal timing must be correct. Software utilities are available from Raytheon to set a PC display controller to either NTSC or PAL timing and preserve the settings when an applications program is run. Software also may be used to make slight position corrections, left/right and up/down.

Horizontal timing is important for several reasons. First the image must be correctly positioned. Second, if the TV display contains a comb filter for Y/C separation, then the line period of incoming video must equal the comb delay. (Note that the TV line period from the TMC2361 is double the incoming VGA line period.)

Table 10. VGA Horizontal Timing Parameters

Television Standard	TVSTD1-0	Line Rate (kHz)	Front Porch (pixels)	Horiz Sync (pixels)	Back Porch (pixels)	Active Video (pixels)
NTSC(-EIA)	1x	31.469	18	96	46	640
PAL/B, G, I	01	31.250	18	96	54	640
PAL/M	00	31.469	18	96	46	640

Table 11. VGA Vertical Timing Parameters

Television Standard	TVSTD1-0	Frame Rate (Hz)	Line Rate (kHz)	Full Frame (lines)	Front Porch (lines)	Vert. Sync (lines)	Vsync + Back Porch (lines)	Active Video (lines)
NTSC(-EIA)	1x	59.94	31.469	525	13	2-16	32	480
PAL/B, G, I	01	50	31.250	625	61	2-16	84	480
PAL/M	00	60	31.469	525	13	2-16	32	480

Outgoing TV Formats

Table 7 defines the four different TV formats that may be selected as outputs by the $TVSTD_{1-0}$ inputs.

Tables 12 and Table 13 show the Horizontal and Vertical Timing for the NTSC and PAL formats.

Table 12. NTSC and PAL Horizontal Timing

Television Standard	Field Rate (Hz)	Lines per frame	Line Rate (kHz)	2x pix Rate (MHz)	f_{SC} Freq. (MHz)	Front Porch pixels	Horiz Sync pixels	Back Porch pixels	Active Video pixels	Line H pixels
NTSC and PAL M	59.94	525	15.734	24.546	3.579	18	58	58	646	780
	59.94	525	15.734	27.566	3.579	83	65	83	645	876
PAL	50.00	625	15.625	29.500	4.433	18	70	82	774	944

Table 13. NTSC and PAL Vertical Timing

TV Std	Field Rate (Hz)	Lines per frame	Line Rate (kHz)	Front Porch (lines)	Vertical Sync (lines)	Back Porch (lines)	Active Video (lines)
NTSC	59.94	525	15.734	3-3.5	3	14-14.5	242.5
PAL	50.00	625	15.625	2.5	2.5	21	286.5
PALM	60.00	525	15.734	3	3	14	242.5

Preliminary Information

Timing Diagrams

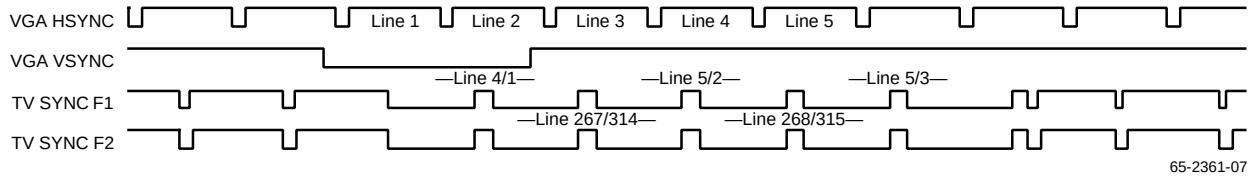


Figure 6. NTSC/PAL Vertical Sync Timing

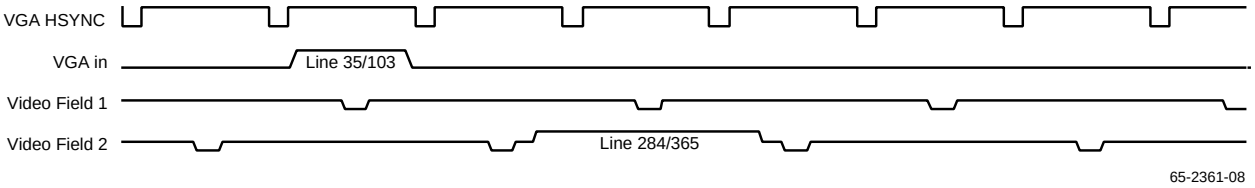


Figure 7. NTSC/PAL, No Filter Timing

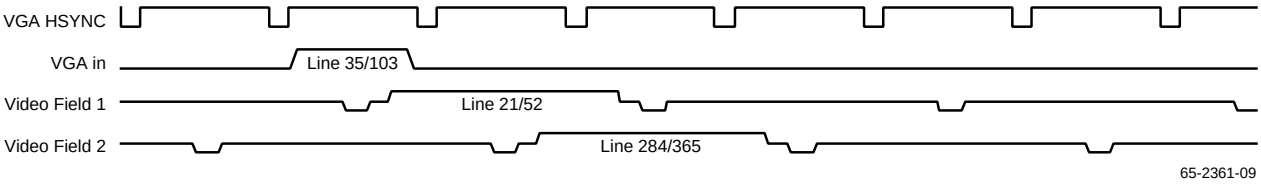


Figure 8. NTSC/PAL, Medium Filter Timing

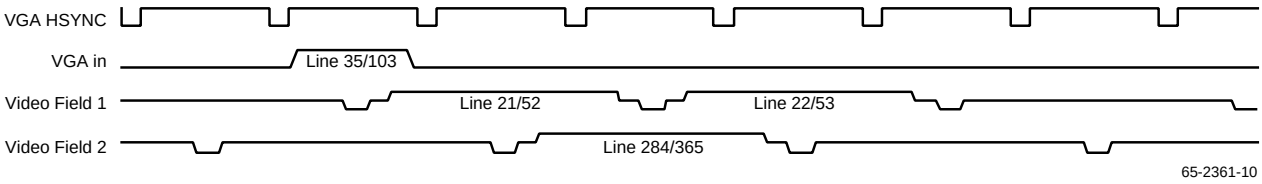


Figure 9. NTSC/PAL, High Filter Timing

Preliminary Information

Equivalent Circuits

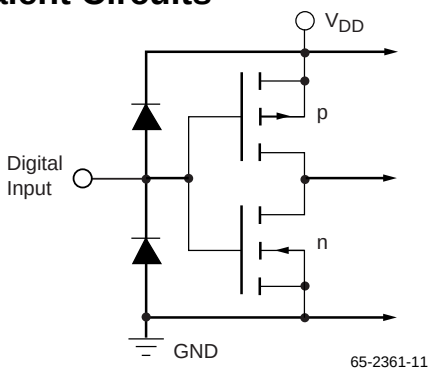


Figure 10. Equivalent Digital Input Circuit

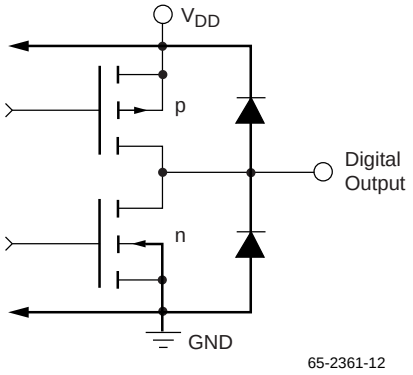


Figure 11. Equivalent Digital Output Circuit

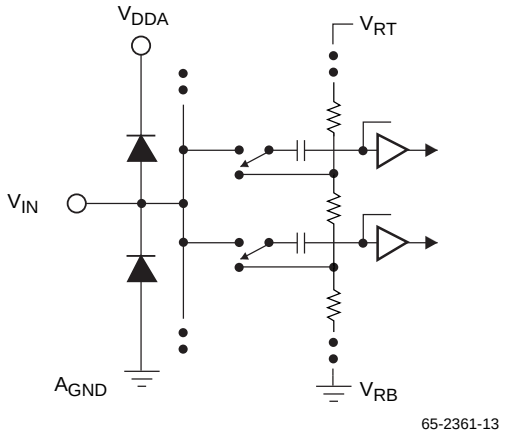


Figure 12. Equivalent A/D Input Circuit

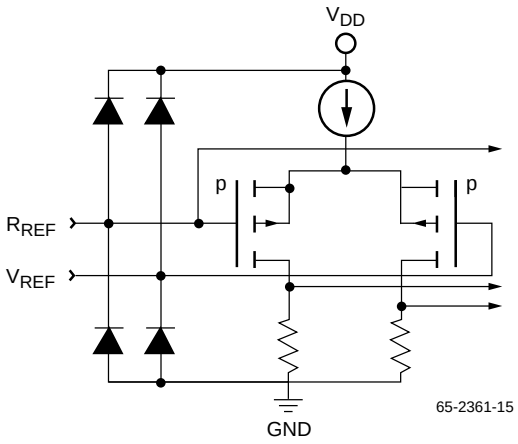


Figure 13. Equivalent D/A Reference Input Circuit

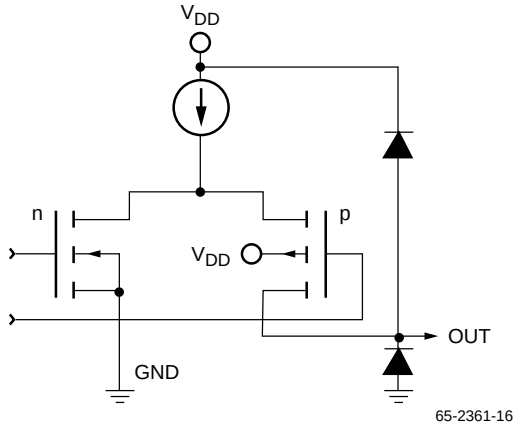


Figure 14. Equivalent D/A Output Circuit

Preliminary Information

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min.	Typ.	Max.	Unit
Power Supply Voltages				
V_{DDPLLA}, V_{DDPLLP}, $V_{DDD/A}$, $V_{DDA/D}$ (Measured to AGND)	-0.5		7.0	V
V_{DD}, V_{DDQ}, (Measured to DGND)	-0.5		7.0	V
$V_{SSD/A}$, $V_{SSA/D}$, V_{SSPLLA}, V_{SSPLLP} (Measured to V_{SS} & V_{SSQ})	-0.5		0.5	V
AGND (Measured to DGND)	-0.5		0.5	V
Digital Inputs				
Applied Voltage (Measured to DGND)[2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Analog Inputs				
Applied Voltage (Measured to AGND)[2]	-0.5		V_{DDA} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Digital Outputs				
Applied Voltage (Measured to DGND)[2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-6.0		6.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Operating, Ambient	-20		110	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C
Electrostatic Discharge[5]			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min.	Nom.	Max.	Units
V_{DD}	Digital Power Supply Voltage	4.75	5.0	5.25	V
V_{DDA}	Analog Power Supply Voltage	4.75	5.0	5.25	V
AGND	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
V_{RT}	Reference Voltage, Top	0.5	0.75	2.0	V
V_{IN}	Analog Input Range	0		V_{RT}	V
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current (I_{REF}= V_{REF}/R_{REF}, flowing out of the R_{REF} pin)		3.15		mA
R_{REF}	Reference Resistor, V_{REF} = Nom		392		Ω
R_L	DAC Total Output Load Resistance		37.5		Ω
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Unit
Power Supply Currents						
I_{DD}	Operating	CVIDEN = H, SVIDEN = H		240	280	mA
I_{DDQ}	Power-Down	$\overline{PWRDN}$ = L		5		mA
Digital Inputs and Outputs						
C_I	Input Capacitance			5	10	pF
C_O	Output Capacitance			10		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{ILP}	Input Current, LOW with pull-up		-70			µA
V_{IHTTL}	Input Voltage, Logic HIGH (TTL)		2.0			V
V_{ILTTL}	Input Voltage, Logic LOW (TTL)				0.8	V
V_{IHCMOS}	Input Voltage, Logic HIGH (CMOS)		3.5			V
V_{ILCMOS}	Input Voltage, Logic LOW (CMOS)				1.5	V
V_{T+}	Schmitt Trigger Positive Threshold			3.0		V
V_{T-}	Schmitt Trigger Negative Threshold			0.8		V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				2.0	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = -2mA	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = 2mA			0.4	V
Analog Inputs						
C_{AI}	A/D Input Capacitance	ADCLK = LOW ADCLK = HIGH		4 12		pF pF
R_{IN}	A/D Input Resistance		500	1000		kΩ
I_{CB}	A/D Input Current				±15	µA
Analog Outputs						
V_{OC}	Video Output Compliance		-0.4		2	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	C_{OUT} = 0 mA, Freq. = 1 MHz		15		pF
V_{RO}	Voltage Reference Output	Internal Reference	0.988	1.235	1.482	V
I_{RO}	VREF Output Current	External VREF	-170		+60	µA
IOS	Short-Circuit Current		-20		-80	mA

Preliminary Information

Switching Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Unit
Clocks						
f_{CKIN}	Reference Clock Frequency			14.31818		MHz
f_{XTOL}	Reference Clock Frequency Tolerance			50		ppm
t_{PWH}	Reference Clock Pulse Width, HIGH			18.5		ns
t_{PWL}	Reference Clock Pulse Width, LOW			18.5		ns
Syncs						
f_H	VGAHS Frequency	60 Hz Modes	30.840	31.469	32.100	KHz
		50 Hz Modes	30.630	31.250	31.880	KHz
N_H	Lines per VGA frame	60 Hz Modes		525		
		50 Hz Modes		625		
		Tolerance			±0	
t_{PWHS}	VGAHS Pulsewidth		1		8	µs
t_{VS-HS}	VGAVS to VGAHS Delay		0			ns
Controls						
t_{PWH}	$\overline{\text{RESET}}$ Input Pulse Width, HIGH		200			ns
t_{PWL}	$\overline{\text{RESET}}$ Input Pulse Width, LOW		200			ns
Serial Microprocessor Interface						
t_{DAL}	SCL Pulse Width, LOW			1.3		µs
t_{DAH}	SCL Pulse Width, HIGH			0.6		µs
t_{STAH}	SDA Start Hold Time			0.6		µs
t_{STASU}	SCL to SDA Setup Time (Stop)			0.6		µs
t_{STOSU}	SCL to SDA Setup Time (Start)			0.6		µs
t_{BUFF}	SDA Stop Hold Time Setup			1.3		µs
t_{DSU}	SDA to SCL Data Setup Time			300		ns
t_{DHO}	SDA to SCL Data Hold Time			300		ns

System Performance Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Unit
A/D Converter Input						
RES_{AD}	A/D Converter Resolution			6		Bits
E_{OTR}	Offset Voltage, Top, Red	R_T–V_{IN} for most positive code transition		70		mV
E_{OTG}	Offset Voltage, Top, Green			40		mV
E_{OTB}	Offset Voltage, Top, Blue			29		mV
E_{OBR}	Offset Voltage, Bottom, Red	V_{IN} for most negative code transition		93		mV
E_{OBG}	Offset Voltage, Bottom, Green			66		mV
E_{OBB}	Offset Voltage, Bottom, Blue			6		mV
D/A Converter Output						
RES_{DA}	D/A Converter Resolution		9	9	9	Bits

Notes:

1. Values shown in Typ column are typical for V_{DD} = V_{DDA} = +5V and T_A = 25˚C.

Application Notes

Circuit Example – PC

Figure 17 is a suggested schematic for the TMC2361 for use in conjunction with a graphics controller located on a VGA controller board. RGB video signals and the vertical and horizontal sync signals are intercepted by tapping outgoing connections to the VGA connector. Control of the TMC2361 is through the serial interface. S-video and CVBS outputs are fed to connector that should be located at the board edge. Power is derived from 5 volt analog and digital supplies. It is recommended that the analog supply be clean of noise.

An optional low pass video filter removes steps from the CVBS output. No sinx/x correction is incorporated since the loss with 2x oversampling D/A converters is only 1 dB for high video frequencies. Schottky diode clamps protect the TMC2361 from high voltage transients.

Video filter characteristics are shown in Figures 15 and 16.

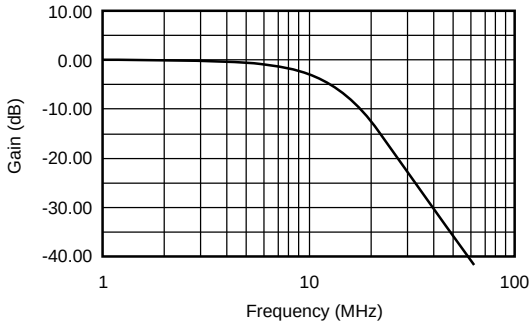


Figure 15. Video Filter Response

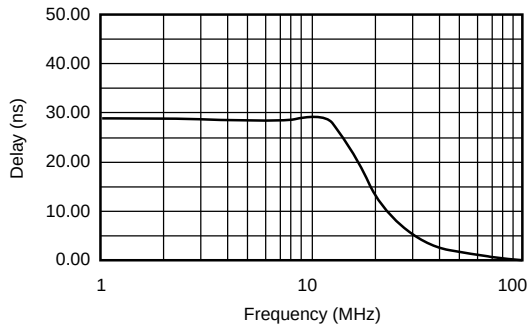


Figure 16. Video Filter Delay

Preliminary Information

V_{TIN} is derived from the bias voltage across R_{REF} which is established by the internal reference voltage available at V_{REF}. R_{REF} is split into two resistors with series resistance to set the R_{REF} current and ratio to establish the V_{TIN} voltage. R_{REF} = 392Ω for a 37.5Ω load.

Power and Ground

Within the TMC2361, separate power is routed to functional sections: A/D converters, phase locked loops, D/A converters, digital processors and digital drivers. All ground pins should be connected to a common ground plane. Power pins should be segregated into analog and digital sections.

Clean analog power should be applied to the V_{DDADC}, V_{DDPLL}, and V_{DDDAC} pins. A 0.1 µF capacitor should be placed adjacent to each group of pins. Chip capacitors are recommended.

Digital power may be derived from system digital +5 volts. If necessary insert a ferrite bead in series with the supply trace. A 47 µF capacitor should be placed close to V_{DDD} pins. At least one 0.1 µF capacitor should be located near V_{DDD} pins to supply transient currents.

Printed Wiring Board Layout

Overall system performance is strongly influenced by the PWB design. Layout and connection principles are embodied in Figure 18. PWB design tips are:

1. Locate the TMC2361 circuit near the board edge, near to video output connectors.
2. Route analog traces over the ground plane.
3. Position localized components, such as phase locked loop filters and reference resistors close to the TMC2361.
4. If a crystal oscillator is used locate the package close to the TMC2361. If a remote clock is used, make the trace connection a transmission line and terminate 330/220 ohm or equivalent to match line impedance.
5. Cleanly route RGB inputs to the TMC2361 treating connection as transmission lines and segregating video traces from digital connection or areas of noise.
6. Tightly group the components for each CVBS or S-video filter. Keep the path between the filters and the CVBS and S-video connectors short.
7. Use a separate power planes for the TMC2361. Separate analog and digital power planes or use individual traces to connect power.

Circuit Example – TV

Figure 19 depicts a recommended circuit for TV which is similar to the Display Controller version described above. Similar principles of operation apply with only slight changes. In this example, direct control through pins is shown. Control through the serial bus is an alternative.

It is no longer practical to tap the VGA source. Instead, a cable connects RGB, HSYNC and VSYNC to a VGA connector on the TMC2361 PWB. RGB lines must be terminated with 75Ω loads.

Video quality can be optimized by connecting the S-video output of the TMC2361 to the luminance and chrominance (Y/C) inputs within the TV chassis. This approach eliminates composite video artifacts such as herringbone distortion and hanging dots that are caused by the TV decoder. Low pass filters may be omitted from the Y/C channels since the bandwidth of the TV amplifiers will eliminate aliasing effects. Protection diodes are not required because the Y/C connection is controlled.

With short Y/C connections. R_{REF} = 787Ω for a 75Ω loads.

Layout principles follow the PC design approach.

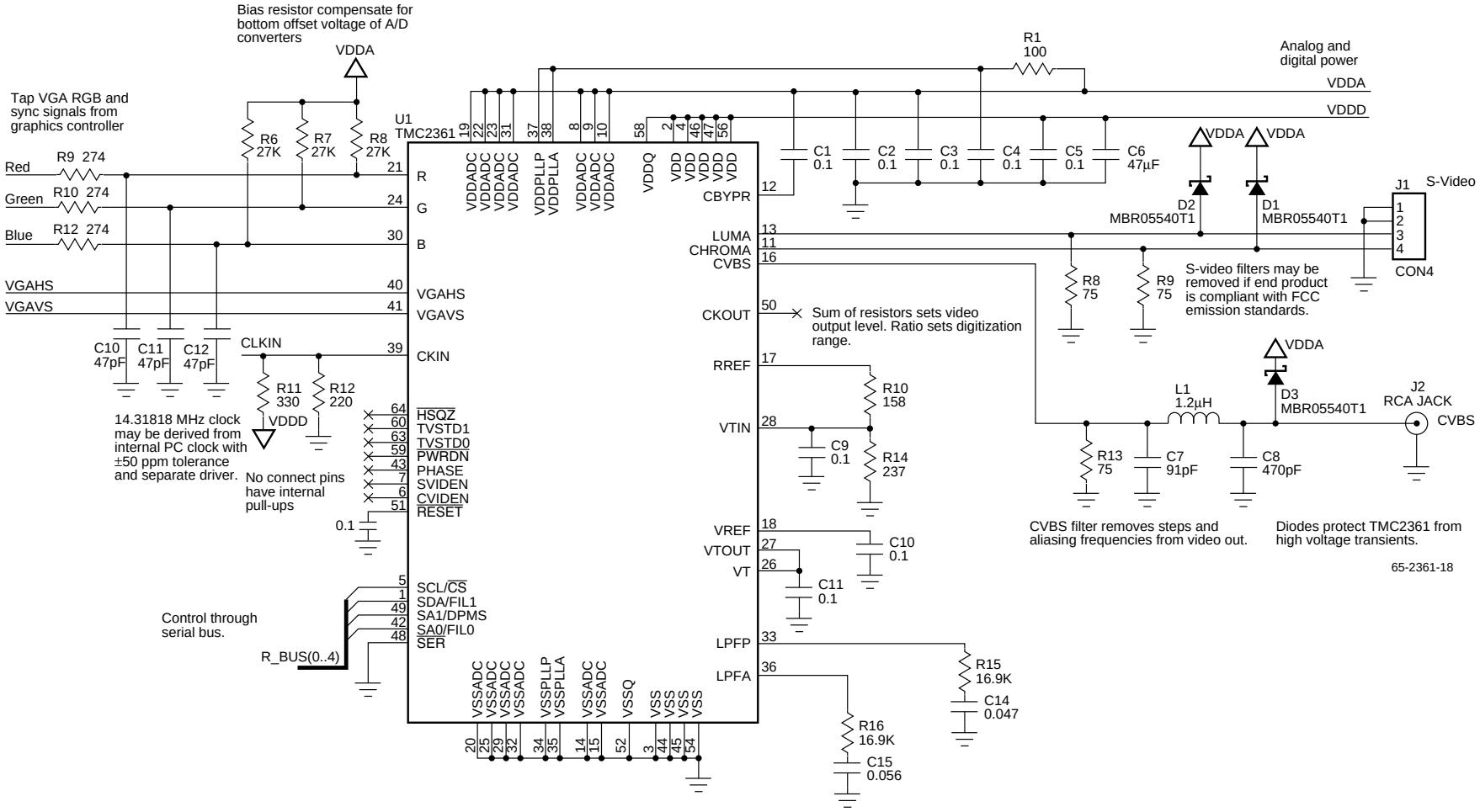


Figure 17. TMC2361 Configuration for Display Controller

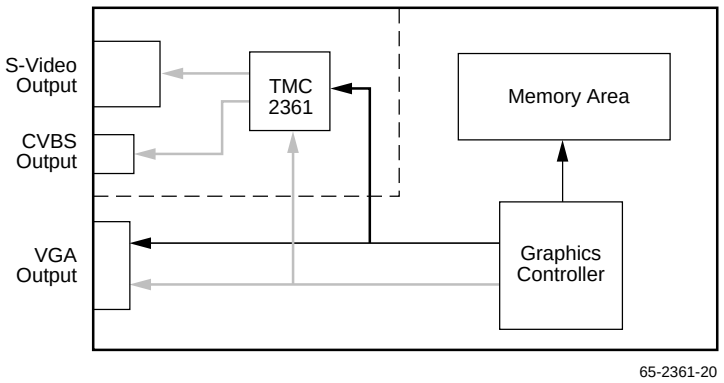


Figure 18. Layout, Connection and Power Distribution Strategy

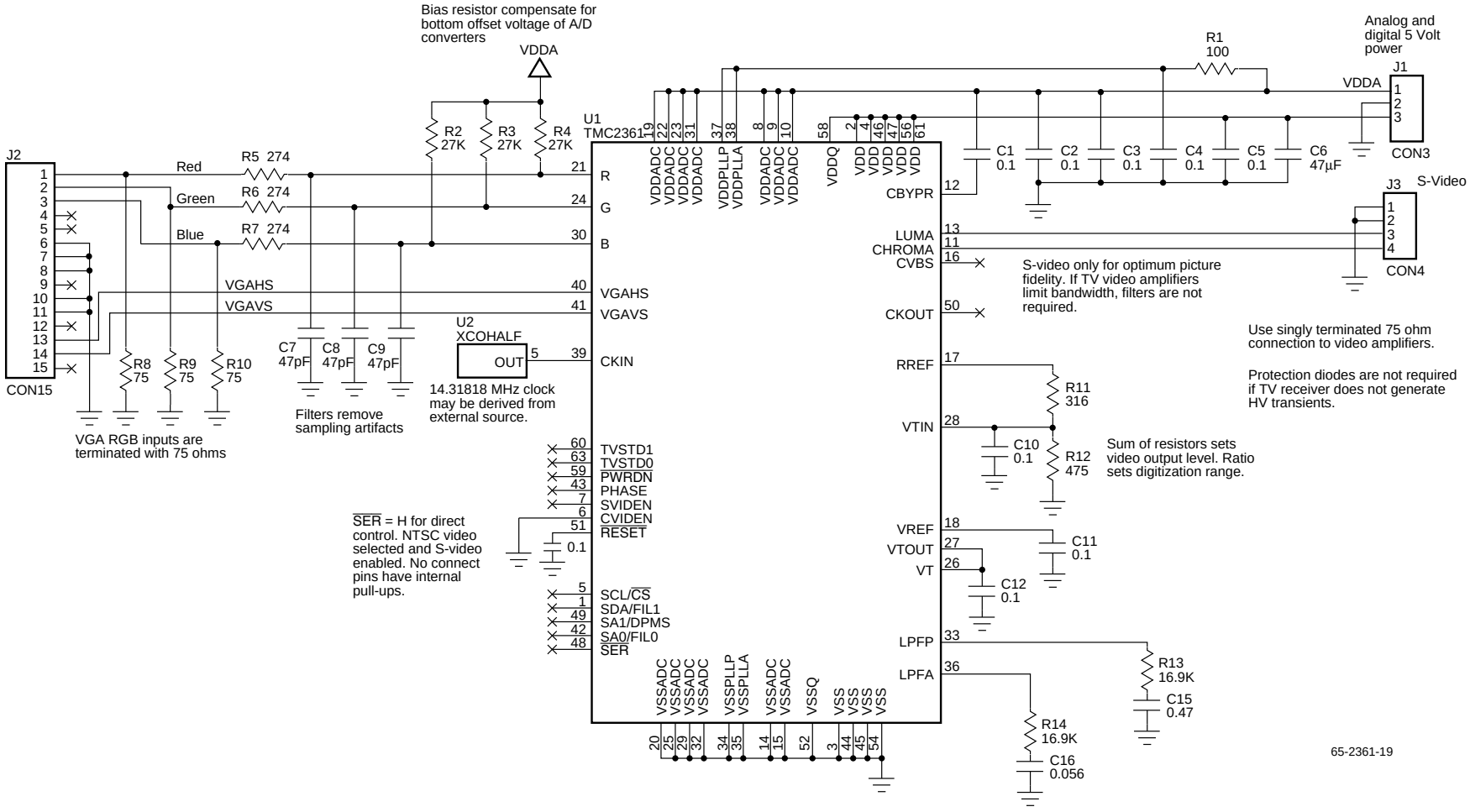


Figure 19. TMC2361 Configuration for TV

Notes:

Notes:

Notes:

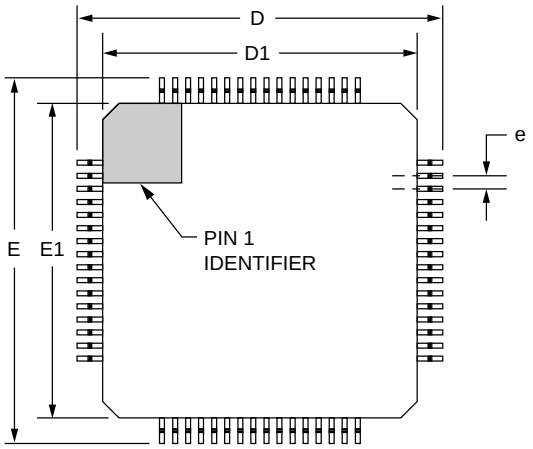
Mechanical Dimensions

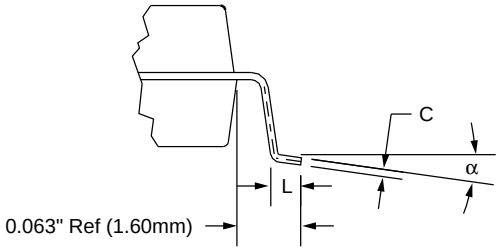
64-Lead MQFP Package

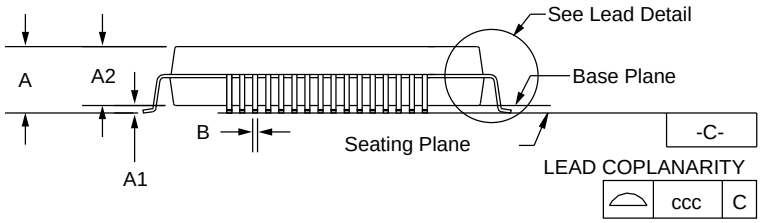
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.096	—	2.45	
A1	.010	—	.25	—	
A2	.077	.083	1.95	2.10	
B	.012	.018	.30	.45	7
C	.005	.009	.13	.23	
D/E	.667	.687	16.95	17.45	
D1/E1	.547	.555	13.90	14.10	2
e	.0315 BSC		.80 BSC		
L	.029	.041	.73	1.03	6
N	64		64		4
ND	16		16		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion.
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. "B" includes lead finish thickness.







Preliminary Information

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2361KPC	0°C to 70°C	Commercial	64 Lead MQFP	2361KPC

Preliminary Information

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